UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,535	06/27/2001	Jeom Jae Kim	8733-459.00	3210

30827 7590 02/19/2004

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,535	KIM ET AL.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,19-25 and 34-37* is/are pending in the application.

4a) Of the above claim(s) *36 and 37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,19-25,34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action responds to the Amendment filed 21 November 2003.

Election/Restrictions

1. Newly submitted claims 36 and 37 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The originally presented claims are drawn to an LCD with a single short prevention member formed on the insulating layer and above the first electrode pattern (gate line, gate electrode, and lower storage capacitor electrode). New claims 36 and 37 are drawn to an LCD with an additional non-specific short prevention member which is a different species than previously claimed.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 36 and 37 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **19**, 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,072,550 (**Kim**).

Regarding claim 19, **Kim** discloses a method of fabricating a liquid crystal display device, comprising:

forming a gate line **11**, **111** on a first substrate **100** having a pixel area (Figs. 4 and 6);

forming an insulating layer **112** over the first substrate **100** and over the gate line **11**, **111**;

forming a short-prevention member **113** on the insulating layer **112** and over an edge of the gate line **11**, **111** (Figs. 4 and 6);

forming a data line **14**, **15**, **16** on the insulating layer **112**; and

forming a pixel electrode **23** in the pixel area.

It is seen to be inherent that semiconductor region **113** of **Kim** is the short-prevention member and prevents electric shorts in the data line pattern **14**, **15**, **16** by Applicant's own admission in the specification. The instant specification states that when the semiconductor layer extends beyond the gate and gate insulating region, no residual short-causing conductive material build up in the edge regions (p. 8, lines 1-12; Figs. 3 and 4). Because the semiconductor region **113** in **Kim** extends beyond the gate electrode in edge regions where residue would form, no residue will be formed in this area along the edge region of the electrode pattern and accordingly, no short can form in this area. (See MPEP 2112.)

Regarding claim 22, the gate electrode **111** is formed under the insulating layer **112**; the semiconductor layer **113** is formed over the insulating layer **112**; and the source/drain electrodes **15**, **16** are formed over the semiconductor layer **113** (Figs. 4 and 6).

Regarding claim 23, the short-prevention member **113** is formed of a same material as the semiconductor layer **113**.

Regarding claim 24, the short-prevention member **113** is formed as an island (Fig. 4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1**-10, 20, 21, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kim** in view of Applicant's admitted prior art (**APA**).

Regarding claim 20, **Kim** discloses that the gate line **11** includes a gate electrode **111**, but does not state that the gate line includes a lower electrode of a storage capacitor.

APA teaches that it is conventional in the art to form a first electrode pattern (i.e. a gate line pattern) having a lower electrode of a storage capacitor. (See instant specification p. 3, first paragraph.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form a lower electrode of a storage capacitor in the gate line pattern of **Kim** in order to form a storage capacitor and because **APA** teaches that this is conventional in the art and would save time and money by preventing the performing of additional steps to form a storage capacitor.

Then the only difference is that **Kim** does not indicate the method of patterning the gate line pattern is by wet etching.

APA teaches that it is conventional to wet etch metal patterns to for electrode patterns in the production of LCDs. (See instant specification p. 3, lines 16-20.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use wet etching as the method of patterning the gate line pattern in **Kim**, because **Kim** is silent to the method by which the patterning is carried out, such that one of ordinary skill would be motivated to use conventional methods, such as wet etching, as taught by **APA**.

Regarding claim 21, **Kim** discloses that the data line pattern includes a data line **12** and source/drain electrodes **15**, **16**, but does not state that the data line pattern includes an upper electrode of a storage capacitor.

APA teaches that it is conventional in the art to form a data line pattern having an upper electrode of a storage capacitor. (See instant specification p. 3, lines 11-15.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form an upper electrode of a storage capacitor in the data line pattern of **Kim** in order to form a storage capacitor and because **APA** teaches that this is conventional in the art and would save time and money by preventing the performing of additional steps to form a storage capacitor.

Then the only difference is that **Kim** does not indicate the method of patterning the data line pattern is by wet etching.

APA teaches that it is conventional to wet etch metal patterns to for electrode patterns in the production of LCDs. (See instant specification p. 3, lines 16-20.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use wet etching as the method of patterning the data line pattern in **Kim**, because **Kim** is silent to the method by which the patterning is carried out, such that one of ordinary skill would be motivated to use conventional methods, such as wet etching, as taught by **APA**.

Regarding claims **1**-5 and 7-9, **Kim**, as explained above, discloses each of the claimed features except for indicating that there exists residual material on the edge of the data line pattern.

APA teaches that residue material is left as a matter of wet etching the gate electrode. (See instant specification p. 3, lines 16-20.)

It would have been obvious for one of ordinary skill in the art at the time of the invention to wet etch the data line pattern of **Kim**, as noted above with regard to claim 21, and accordingly, the residual material would be left on the edge portion wherever the short prevention (i.e. the amorphous silicon layer **113**) layer of **Kim** is not found.

Regarding claim 6, although this claim has no patentable weight since it is a product-by-process claim, **Kim** nonetheless discloses that the short-prevention member is formed at a same time as the semiconductor layer **113** because the semiconductor layer and the short-prevention layer are integral --just as in the instant application.

Regarding claim 10, it is seen to be inherent that discloses that the LCD in **Kim** further includes a second substrate adjacent the first substrate; and a liquid crystal between the first substrate and the second substrate, as it would not be an LCD, otherwise, as admitted to in the instant specification p. 2, lines 17-19.

Regarding claims 34 and 35, **Kim** discloses that the short prevention member **113** is formed over the edge of the gate electrode **111** (Kim, Figs. 4 and 6).

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kim** in view of US 5,060,036 (**Choi**).

The prior art of **Kim**, as explained above, discloses each of the claimed features except for indicating that the short-prevention layer (i.e. the amorphous silicon layer **113**) is formed by dry etching.

Choi teaches a method of forming the silicon active region of a TFT for a LCD wherein **Choi** indicates that it is known to pattern the amorphous silicon active region using dry etching (col. 2, lines 41-47).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use dry etching to pattern the short-prevention member (i.e. the amorphous silicon layer **113**) of **Kim** using dry etching, because **Kim** is silent to the method of patterning, such that one of ordinary skill would use a well known etching method for amorphous silicon already proven successful for use in TFT fabrication for LCDs, such as that taught to be conventional in **Choi**.

Response to Arguments

7. Applicant's arguments filed 21 November 2003 have been fully considered but they are not persuasive.

Applicant argues that neither Kim nor Kim in view of APA discloses the short prevention member. Examiner respectfully disagrees. Kim discloses a short prevention member 113 inherently. Applicant fails to meet the required burden of proof as required by the precedent cited in MPEP 2112. In other words, Applicant has the burden of disproving that the feature shown in Kim does not prevent shorts. To make such assertion, however, would only prove that the instant invention is not enabled, since the feature 113 in Kim meets all requirements in the instant specification for providing short prevention.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erik Kielin
Primary Examiner
9 February 2004